Application No. 10/614503
Office Action: mailed May 20, 2004
Amndt.dated: August 2, 2004

REMARKS/ARGUMENTS:

Claims 31, 34 and 36 have been amended; no claims have been cancelled and no new claims have been added. Claims 21-39 are pending in this application.

The specification has been amended to update the information concerning related applications.

Claims 31, 34 and 36 have been amended to meet the objections raised in paragraph 3 of the Office Action and are believed to be allowable as indicated in paragraph 8 of the Office Action.

Claim rejections under 35 US 102(b)

Claims 21-23 and 25-27 were rejected as anticipated by US Patent 5,218,704 (Watts, Jr.). The rejection is respectfully traversed.

To anticipate a claim under 35 US 102, a reference must disclose each and every feature as recited in the claim under rejection. Watts fails to meet this standard because Watts Jr does not monitor a "time related level of processing activity" of his CPU. Watt explicitly discloses that his CPU is placed into a low power mode in response to instantaneous recognition of an IDLE or "do nothing" state: "IDLE branch 60 (more specifically set out in FIG. 2b) is executed by a hardware or software interrupt for an IDLE or "do nothing" function. This type of interrupt is caused by the CPU entering either an IDLE or "do nothing" loop (i.e. planned inactivity)." Col. 6, lines 37-49. Watts power conservation monitor 40 checks a variable "Idle-tick" which "refers to the number of interrupts found in a 'do nothing' loop." (Col 7, lines 17-19). Watts teaches that in execution of the IDLE loop 60 (Fig. 2b, col. 7, line 35 *et seq.*), if a state "Idle_tick equals IDLE_MAXTICKS" is detected (Fig. 2b, 200) and "Power_level" does not equal zero (Fig. 2b, 230) and if interrupts are available (Fig. 2b, 240) then a SAVE POWER subroutine (Fig. 2b, 250) is executed and the CPU clock is stepped down to a sleep level for the duration of the SAVE POWER subroutine 250 (Fig. 2b, col. 8, lines 32-40 and Fig. 2c)).

Thus, Watts Jr. teaching is limited to power conservation monitor response to an instantaneous recognition of an IDLE state and , subject to certain qualifications, to place the CPU into a low power mode which is clearly not a "time related level of . . . activity" and is differentiated from:

"monitoring a time related level of processing activity by a processing unit including a processor"

as set forth in claims 21 and 25, and

"monitoring a time related level of processor activity in a CPU"

as set forth in claim 34.

Thus, it is not seen that Watts Jr monitors a "time related level of processing activity" of his CPU but rather only monitors occurrence of an IDLE state as one factor required to initiate a "SAVE POWER" subroutine. Watts Jr. fails to anticipate any of claims 21-23 and 25-27.

Claim rejections under 35 USC 103

Claims 24 and 28-30 were rejected under 35 US 103(a) as unpatentable over Watts Jr. in view of US Patent 4670837 (Sheets). The rejection is respectfully traversed based on the deficiencies of Watts Jr. discussed above. Moreover, Sheets does not teach the monitoring feature of claim 24, as asserted by the Examiner; to the contrary, Sheets states that a consequence of reducing clock frequency is to reduce "the power consumed by the microprocessor 101 and, by reducing the required access rate to the associated devices, i.e. ROM 107, RAM 108, and I/O port 109, also reduces the power consumed by those devices." Further, Watts teaches instantaneous response to an IDLE state by reducing power only for the duration of a "do nothing" loop – see Watts, Jr. col. 3, lines 43-45, col. 4, lines 22-24, col. 5, lines 54-61, col. 8, lines 32-40. Sheets teaching directed "determining the processing load presented to the system and then reducing the clock frequency at which the load is driven, during times when the processing load is reduced." -col. 1, lines 45-54- is not seen to be compatible with the principle of operation taught by Watts, Jr.. Withdrawal of the rejection of claims 24 and 28-30 is requested together with allowance of those claims.

Regarding Paragraph 9 of the Office Action, documents U and V have publication dates later than the December 17, 1991 filing date of application N. 07/809,301 from which the present application derives priority under 35 USC 120, and thus are not prior art with respect to the present application.

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It is believed that all pending claims are in condition for allowance and early action to that effect is solicited. If there are any issues that could be resolved by discussion, a telephone call to the undersigned attorney at (972) 862-7428 would be appreciated.

Date: August 2, 2004
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Respectfully submitted,

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